YIELD OPTIMIZATION OF NONLINEAR CIRCUITS WITH STATISTICALLY CHARACTERIZED DEVICES

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ABSTRACT

A comprehensive treatment of yield optimization of nonlinear microwave circuits with statistically characterized devices is proposed. We fully exploit advanced techniques of one-sided ℓ_1 circuit centering with gradient approximations, and efficient harmonic balance simulation with exact Jacobians. Multidimensional statistical distributions of the intrinsic and parasitic parameters of FETs are fully handled. Yield is driven from 25% to 61% for a frequency doubler design having 34 statistically toleranced parameters. Yield of a small-signal amplifier is increased from 36% to 68%.

INTRODUCTION

Yield optimization [1-3] has been extensively explored in the literature. For linear circuits, it is currently finding its way into commercial microwave CAD software. Yield optimization of practical nonlinear microwave circuits remains unaddressed hitherto.

Requirements essential to yield optimization of nonlinear microwave circuits are: (1) effective approaches to design centering, (2) highly efficient optimization techniques, (3) fast and reliable simulation, (4) flexibility of handling various statistical representations of devices and elements, and (5) low design costs and short design cycles.

In this paper, we offer an approach for efficient yield-driven optimization of nonlinear microwave circuits with statistically characterized devices. The formulation of the yield problem for nonlinear circuits is described. A powerful and robust one-sided ℓ_1 optimization algorithm for design centering recently proposed by Bandler et al. [3, 4] is adopted. An effective gradient approximation technique presented by Bandler et al. [5] is integrated with the one-sided ℓ_1 algorithm to handle inexact gradients. The harmonic balance method is implemented with exact Jacobian matrices for fast convergence and improved robustness. Independent and/or correlated normal distributions and uniform distributions describing large-signal FET model parameters and passive elements are fully accommodated.

The yield optimization of a microwave frequency doubler with a large-signal statistically simulated FET model is successfully carried out. The performance yield was increased from 25% to 61%. We believe that this is the first demonstration of yield optimization of nonlinear circuits operating under large-signal steady-state periodic or almost periodic conditions.

We also consider a small-signal amplifier. The harmonic balance method enables us to simulate the small-signal linearized circuit under variable DC bias conditions and, consequently, to study the effects of operating conditions on performance yield of the circuit. The yield of the amplifier was increased from 36% to 68%.

FORMULATION OF THE YIELD PROBLEM FOR NONLINEAR CIRCUITS

In yield estimation and statistical circuit design, a set of outcomes around the given nominal design ϕ^0 is considered. These outcomes are sampled according to the element statistics including possible correlations and are denoted by ϕ^i, i = 1, 2, ... , N.

Suppose that the number of harmonics considered in simulation is H. Specifications are given at the DC level and/or several harmonics. Suppose that specifications are applied to circuit responses at the kth harmonic. The set of specifications and the corresponding set of calculated response functions of the outcome, ϕ^i, are denoted by

$$S_j(k), \quad 0 \le k \le H, \quad j = 1, 2, ..., M \tag{1}$$

and

$$F_j(\phi^i, k), \quad 0 \le k \le H, \quad j = 1, 2, ..., M, \tag{2}$$

where M is the number of specifications. The error functions for the ith outcome, $e(\phi^i)$, comprise the entries

$$F_j(\phi^i, k) - S_{uj}(k), \tag{3}$$

and/or

$$S_{lj}(k) - F_j(\phi^i, k), \tag{4}$$

where $S_{uj}(k)$ and $S_{lj}(k)$ are upper and lower specifications. Responses involving more than one harmonic such as conversion gain or power added efficiency can be similarly handled.

An outcome ϕ^i represents an acceptable circuit if all entries in $e(\phi^i)$ are nonpositive. Yield can be estimated by

$$Y \approx N_{pass}/N, \tag{5}$$

where N_{pass} is the number of acceptable circuits and N is the total number of circuit outcomes.

YIELD OPTIMIZATION

The formulation of the objective function for our yield optimization approach consists of two steps. First, the generalized ℓ_1 function $v(e(\phi^i))$ can be calculated from $e(\phi^i)$ [3]. Then, the one-sided ℓ_1 objective function of yield optimization [3] is defined by

$$u(\phi^0) = \sum_{i \in J} \alpha_i v(e(\phi^i)), \tag{6}$$

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where $J = \{i \mid v(e(\phi^i)) > 0, i = 1, 2, ..., N\}$ and α_i are properly chosen non-zero multipliers. Only positive error functions of individual outcomes contribute to the overall objective function. The highly efficient optimization algorithm of [4] is used to minimize $u(\phi^0)$, achieving a centered design with improved yield.

Since the one-sided ℓ_1 algorithm requires gradients, the flexible and effective gradient approximation algorithm proposed in [5] is modified here to address the fact that analytical gradients are traditionally not produced by general purpose large-scale simulators of nonlinear circuits.

HARMONIC BALANCE METHOD AS SIMULATION TOOL

Responses of nonlinear circuits operating in a periodic steady-state regime are calculated by the harmonic balance method. In statistical design, the circuit simulation accounts for an extremely large portion of the overall computational effort, because of the large number of outcomes simulated individually. The notable difference between linear and nonlinear simulations is that the harmonic balance method is an iterative process. To achieve fast convergence and reliable solutions, our program calculates exact Jacobian matrices.

STATISTICAL OUTCOMES

Purviance et. al. [6] treated the statistical characterization of small-signal FET models. Our proposed yield optimization requires statistically described large-signal FET models. We use a random number generator capable of generating statistical outcomes from the independent and multidimensional correlated normal distributions and from uniform distributions.

Parameters of the nonlinear large-signal models have certain physical limits. A normal distribution random generator may generate outcomes far beyond these limits. Such outcomes must be carefully detected and eliminated.

A FET FREQUENCY DOUBLER EXAMPLE

Consider the FET frequency doubler example shown in Fig. 1 used by Microwave Harmonica [7]. It consists of a common-source FET with a lumped input matching network and a microstrip output matching and filter section. The fundamental frequency is 5GHz. Let $CG(\phi,2,1)$ be the conversion gain between input port at fundamental frequency and the output port at the second harmonic. Let $SP(\phi,2)$ be the spectral purity of the output port at the second harmonic. The design specifications are 2.5 dB for the conversion gain and 19 dB for the spectral purity. The error functions are

$$e_1(\phi) = 2.5 - CG(\phi,2,1)$$

and

$$e_2(\phi) = 19 - SP(\phi,2).$$

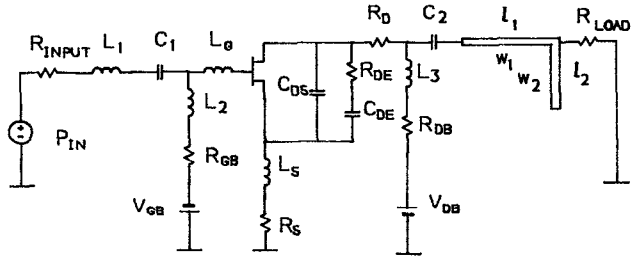

Fig. 1 Circuit diagram of the FET microwave frequency doubler example. The nominal values for non-optimization variables are: L_2 = 15nH, L_3 = 15nH, C_1 = 20pF, C_2 = 20pF, $w_1 = 0.1\times10^{-3}$m, $w_2 = 0.635\times10^{-3}$m, $R_{LOAD} = R_{INPUT} = 50\Omega$, and $R_{GB} = R_{DB} = 10\Omega$.

The optimization variables include the input inductance L_1 and the microstrip lengths l_1 and l_2. The operating condition of a frequency doubler is essential for its performance. Therefore, two bias voltages, V_{GB} and V_{DB}, and the driving power level, P_{IN} are also considered as optimization variables.

The intrinsic large-signal FET model is the modified Materka and Kacprzak model [7]. Independent uniform distributions are assumed with fixed tolerances of 3% for P_{IN}, V_{GB}, V_{DB}, L_1, l_1, and l_2. Independent uniform distributions are assumed with fixed tolerances of 5% for L_2, L_3, C_1, C_2, w_1 and w_2. Normal distributions are assumed for all FET intrinsic and extrinsic parameters. The standard deviations of these distributions are listed in Table I. The correlation parameters are assumed based on [6]. Certain modifications have been made to adjust our large-signal parameter correlations to be consistent with the small-signal FET model dealt with in [6].

TABLE I
ASSUMED STATISTICAL DISTRIBUTIONS FOR THE FET PARAMETERS

FET Parameter	Nominal Value	Standard Deviation	FET Parameter	Nominal Value	Standard Deviation
L_G(nH)	0.16	5%	S_I	0.676×10^{-1}	0.65%
$R_D(\Omega)$	2.153	3%	K_G	1.1	0.65%
L_S(nH)	0.07	5%	τ(pS)	7.0	6%
$R_S(\Omega)$	1.144	5%	S_S	1.666×10^{-3}	0.65%
$R_{DE}(\Omega)$	440	14%	I_{G0}(A)	0.713×10^{-5}	3%
C_{DE}(pF)	1.15	3%	α_G	38.46	3%
C_{DS}(pF)	0.12	4.5%	I_{B0}(A)	-0.713×10^{-5}	3%
I_{DSS}(A)	6.0×10^{-2}	5%	α_B	-38.46	3%
V_{p0}(V)	-1.906	0.65%	$R_{10}(\Omega)$	3.5	8%
γ	-15×10^{-2}	0.65%	C_{10}(pF)	0.42	4.16%
E	1.8	0.65%	C_{F0}(pF)	0.02	6.64%

The following parameters are considered as deterministic: $K_E = 0.0$, $K_R = 1.111$, $K_I = 1.282$, $C_{1S} = 0.0$, and $K_F = 1.282$. For definitions of the FET parameters, see [8].

The starting point for yield optimization is the solution of the conventional nominal design w.r.t. the same specifications, using L_1, l_1 and l_2 as optimization variables. The initial yield based on 500 outcomes is 24.8%. 50 statistically selected outcomes are used in the yield optimization process. The solution found by our approach improves the yield to 57%. Then another set of 50 outcomes is selected and optimization restarted. After this, the final yield is 61.4%. Computational details are given in Table II. Figs. 2 (a) and (b) show histograms of the conversion gain before and after yield optimization. Before yield optimization, the center of the distribution is on the left-hand side of the design specification of 2.5 dB, indicating that most outcomes are unacceptable. After yield optimization, the center of the distribution is shifted to the right-hand side of the 2.5 dB specification. Most outcomes then satisfy the specifications.

TABLE II
YIELD OPTIMIZATION
OF THE FET FREQUENCY DOUBLER

Variable	Starting Point	Nominal Design	Solution I	Solution II
P_{IN}(W)	2.0000×10^{-3}*	2.0000×10^{-3}	2.5000×10^{-3}	2.4219×10^{-3}
V_{GB}(V)	-1.9060*	-1.9060	-1.9010	-1.9011
V_{DB}(V)	5.0000*	5.0000	4.9950	4.9949
L_1(nH)	1.0000	5.4620	5.4670	5.4670
l_1(m)	1.0000×10^{-3}	1.4828×10^{-3}	1.6306×10^{-3}	1.7088×10^{-3}
l_2(m)	5.0000×10^{-3}	5.7705×10^{-3}	5.7545×10^{-3}	5.7466×10^{-3}
Yield		24.8%	57.0%	61.4%
No. of Optimization Iterations			11	8
No. of Function Evaluations			41	26

* Not considered as variables in nominal design.
The yield is estimated from 500 outcomes.

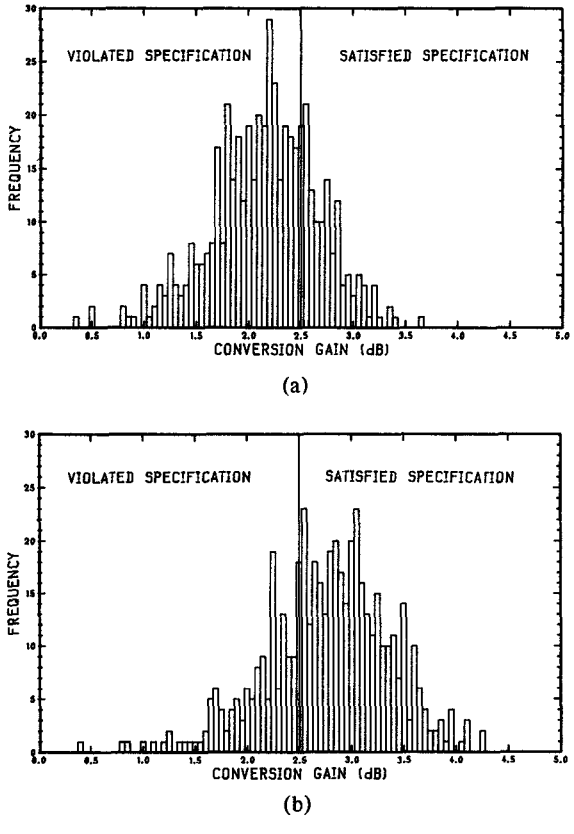

Fig. 2 Histogram of conversion gains of the frequency doubler based on 500 statistical outcomes, (a) before and (b) after yield optimization. The center of the distribution is moved from the left hand side of the specification shown by a vertical line to the right hand side.

A FET AMPLIFIER EXAMPLE

The circuit considered is shown in Fig. 3. Employing both the DC and fundamental frequency, the harmonic balance method not only solves the small-signal linearized circuit, but also simulates the DC bias condition. We perform a yield optimization allowing the bias voltages to vary during optimization. This enables us to study the effects of operating conditions on performance yield of a linear circuit.

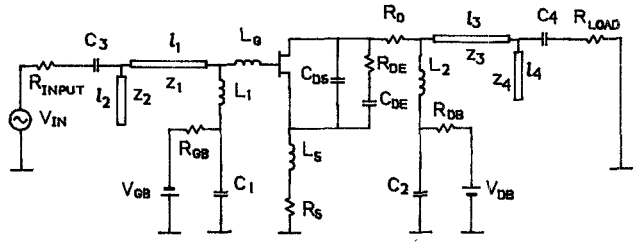

Fig. 3 Circuit diagram of the FET small-signal amplifier example. The nominal values for non-optimization variables are: $C_1 = C_2 = C_3 = 25$pF, $L_1 = L_2 = 100$nH, $R_{LOAD} = R_{INPUT} = 50\Omega$, and $R_{GB} = R_{DB} = 10\Omega$.

Performance specifications are imposed as $|S_{11}| \le$ -6dB, $|S_{22}| \le$ -6dB and 18dB $\le |S_{21}| \le$ 20dB. Totally 9 frequency points were selected from the interval of 3.8GHz ~ 4.2GHz. The FET model and statistics used for this example are the same as those used in the doubler example. The starting point for yield optimization is the solution of conventional nominal design in which two bias voltages are held as constants. Estimated yield at this point is 36%.

In yield optimization, besides two bias voltages, characteristic impedances and electrical lengths of the transmission lines and of the open stubs in the input and output matching networks are also chosen as optimization variables. Independent uniform distributions with 3% tolerances are assumed for V_{GB}, V_{DB}, Z_1, l_1, Z_2, l_2, Z_3, l_3, Z_4, l_4, C_1, C_2, C_3, C_4, L_1, and L_2.

In the first design, 50 statistical outcomes were used. The yield at the solution point is 50%. Then optimization is restarted with 50 outcomes. Yield is improved to 68%.

After yield optimization the bias voltages, V_{GB} and V_{DB}, are changed from -0.95 and 4 to -0.762 and 3.45, respectively. The computational details are listed in Table III. Replacing the short, high impedance transmission line (represented by Z_1 and l_1) by a 3.73nH inductor, we obtain a yield of 71%, which is very close to the yield of the original circuit.

Figs. 4 (a) and (b) show response curves of S_{11} for 50 statistical outcomes before and after yield optimization, respectively. The dense band at the lower frequency region in Fig.4 (a) is pushed below the specification line in Fig. 4 (b), demonstrating that, after yield optimization, more circuit outcomes satisfy the specification on S_{11}.

CONCLUSIONS

The first comprehensive demonstration of yield optimization of statistically characterized nonlinear microwave circuits operating within the harmonic balance simulation environment has been made. Advanced one-sided ℓ_1 design centering combined with efficient harmonic balance simulation using exact Jacobians is exploited. Large-signal FET parameter statistics are fully facilitated. Comprehensive numerical experiments directed at yield-driven optimization of a FET frequency doubler and a small-signal amplifier verify our approach. This success will motivate the development of statistical modeling of nonlinear

TABLE III
YIELD OPTIMIZATION
OF THE FET SMALL-SIGNAL AMPLIFIER

Variable	Starting Point	Nominal Design	Solution I	Solution II
V_{GB}(V)	-0.9500*	-0.9500	-0.9489	-0.7621
V_{DB}(V)	4.000*	4.000	3.920	3.447
$Z_1(\Omega)$	50	601.9**	602.0**	602.0**
$l_1(°)$	50	4.740**	4.772**	4.452**
$Z_2(\Omega)$	50	77.15	77.22	77.46
$l_2(°)$	50	63.02	63.09	63.43
$Z_3(\Omega)$	50	90.76	90.78	90.59
$l_3(°)$	50	31.37	31.43	31.97
$Z_4(\Omega)$	50	49.45	49.43	49.77
$l_4(°)$	50	74.11	74.18	74.68
Yield		35.8%	49.6%	68.4%
No. of Optimization Iterations			8	21
No. of Function Evaluations			30	88

* Not considered as variables in nominal design.
** This transmission line may be replaced by an inductor (see text).
The yield is estimated from 500 outcomes.

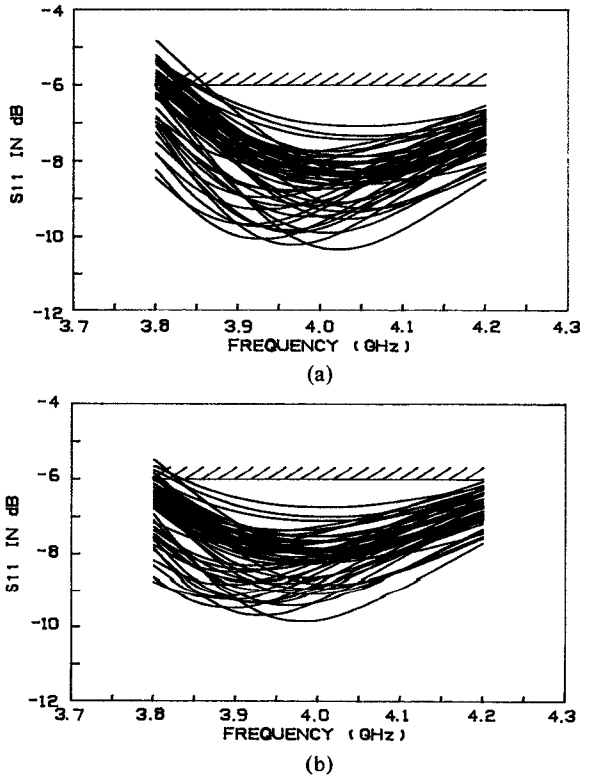

Fig. 4 Response curves of the magnitude of S_{11} for 50 statistical outcomes (a) before and (b) after yield optimization.

microwave devices for large-signal applications.

Modern supercomputers have found applications in microwave CAD [9, 10] with attractive performance-to-cost ratios. Our software has been developed for possible use on supercomputers. The computational performance on the Cray X-MP will be reported in the future.

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